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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Walter Fix et al.

Serial No.:

10/541,957

Filed:

Feb. 2, 2006

Title:

ORGANIC FIELD EFFECT TRANSISTOR AND INTEGRATED CIRCUIT

Examiner:

Swapneel Chhaya

Art Unit: 2822

Atty. Dkt:

411000-138

Customer No. 27162

PROPOSED AMENDED CLAIM 1 UNDER 37 CFR 1.116

19735970250

VIA FAX 571 270 2434 Commissioner for Patents Box 1450 Alexandria, VA 22313-1450

Sir:

This is in response to an Advisory Action dated April 30, 2008 indicating that there are discrepancies in applicants' prior proposed amended claim submitted in view of an examiner's telephone interview with the undersigned on April 22, 2008. the undersigned proposed an amended claim 1 that is believed to overcome the cited reference rejection over Hart as discussed in the interview. Applicants asserted that Hart does not show or suggest the limited overlap or the problem overcome as presently being claimed, calling for:

wherein the second electrode layer completely overlies the current channel and overlies a portion of the source or drain electrodes of the first electrode layer, the overlying portion with respect to the source or drain electrodes having a width solely in the range from about 0 to about 20 µm to thereby minimize parasitic capacitance that otherwise might be present

(The underlined portion was previously at the end of the claim instead of the present location after the term 0 to about 20 µm.)

The examiner misconstrued the meaning of the term "to thereby minimize parasitic capacitance" in the prior response. This is a whereby clause that applies to